WHAT IS CLAIMED IS:

1. A method of defining a phase shifting mask, the method comprising:

defining critical poly regions and adjoining poly, the critical poly regions being regions desired to be defined by phase shifting;

creating phase regions on either side of the critical poly regions;

assigning phase angles to the phase regions such that the phase regions have either a first phase angle or a second phase angle;

defining edges of the phase regions being assigned the second phase angle, the edges not defining a poly pattern;

defining a boundary region around the defined edges; and

defining regions outside a desired poly pattern, phase regions, and boundary region to have the first phase angle, wherein the desired poly pattern, phase regions, and boundary region define a mask.

2. The method of claim 1, further comprising enhancing the phase regions assigned a phase angle.

3. The method of claim 1, wherein enhancing the phase regions assigned a phase angle includes reducing the effect of transition regions by moving transition regions away from the critical poly regions.

6. The method of claim 1, wherein the step of defining a boundary around the defined edges comprises forming a chrome path.

7. The method of claim 1, further comprising defining break locations where phase transitions are most likely to occur.

8. The method of claim 7, wherein the break locations have a width that permits patterning and inspection.

9. The method of claim 1, further comprising generating a trim mask to remove undesired patterns between regions of the first phase angle and the second phase angle.

10. A method of generating phase shifting pattern to improve the patterning of gates and other layers needing sub-nominal dimensions, the method comprising:

defining critical areas;

creating phase areas on either side of the critical areas;

assigning opposite phase polarities to the phase areas on each side of the critical areas;

enhancing phase areas with assigned phase polarities;

defining break regions where phase transitions are likely to occur;

generating polygons to define other edges and excluding the defined break regions;

merging the generated polygons with enhanced critical gate areas having a common phase polarity;

separating the polygons having interactions with more than one polarity into portions which are merged into regions having only one

constructing a boundary region outside of phase 180 regions; and

defining undefined regions as phase 0 regions.

11. The method of claim 10, further comprising:

correcting design rule violations; and

applying optical proximity and process corrections to phase regions to allow proper pattern generation.

12. The method of claim 11, further comprising generating a trim mask to remove undesired patterns between phase 0 and phase 180 regions outside of a desired pattern.

13. The method of claim 12, wherein the generating is done by oversizing boundary and break regions.

14. The method of claim 10, wherein the break regions are about a minimum width of a desired poly pattern.

15. The method of claim 10, wherein enhancing critical areas with assigned phase polarities includes adding edges to the critical areas.

16. A method of enhancing clear field phase shift masks with a border around outside edges, the method comprising:

assigning phase polarities to phase regions;

defining edges of the assigned phase regions;

break regions, wherein the polygons are merged with the assigned phase regions.

18. The method of claim 17, further comprising curing design rule violations and applying correction procedures.

19. The method of claim 17, further comprising generating a trim mask to remove undesired patterns between phase 0 and phase 180 regions.

20. The method of claim 19, wherein the generating is done by oversizing the boundary and break regions.

21. A integrated circuit formed by a process comprising:

defining phase areas including adjoining poly areas located proximate to critical areas;

assigning a first phase angle to the phase areas;

defining remaining poly edges as part of the phase areas;

defining a boundary around the defined phase areas, the areas outside the boundary being assigned a second phase angle, wherein the phase areas, the boundary, and areas outside the boundary defining a mask, wherein the first phase angle and the second phase angle are different;

curing violation areas and applying correction procedures to appropriate areas on the mask; and

patterning a structure on the integrated circuit using the mask.

22. The integrated circuit formed by the process of claim 21, wherein the second phase angle is zero.